Claims 1-30, previously cancelled without prejudice.

31. (Amended) A phase lock loop for providing an output signal with a desired characteristic frequency that is an integer, N, multiple of a characteristic frequency of an input signal, said phase lock loop comprising:

a voltage controlled oscillator generating one or more oscillator signals, wherein each of the one or more oscillator signals are associated with M phases of the desired characteristic frequency of the output signal;

a phase detector for comparing a phase or the frequency characteristic of the input signal to a phase or frequency characteristic of a particular one of the one or more oscillator signals to the input signal; and

a Gray code multiplexer for selecting a particular one of the one or more oscillator signals based on a Gray Code, said Gray code multiplexer further comprising:

a first multiplexer receiving two of the one or more oscillator signals, wherein the two of the one or more oscillator signals have approximately a 180 degree phase shift with respect to each other; and

a second multiplexer receiving another two of the one or more oscillator signals, wherein the another two of

the one or more oscillator signals have approximately a 180 degree phase shift with respect to each other.

32. The phase lock loop of claim 31, further comprising:

a divider circuit for reducing a characteristic frequency of the selected one of the one or more oscillator signals to the desired characteristic frequency.

Claims 33 and 34 previously cancelled without prejudice.

35. (Amended) The phase lock loop of claim 32, further comprising:

one or more divider circuits for reducing the characteristic frequency of at least one of the one or more oscillator signals.

36. (Previously Added) The phase lock loop of claim 35, wherein the one or more divider circuits reduce the frequency characteristic of the at least one of the one or more oscillator signals by an integer, M, factor and an integer, N, factor.

37. (Previously Added) The phase lock loop of claim 31, further comprising:

a loop filter for increasing or decreasing a characteristic frequency of the voltage controlled oscillator signals based on the comparison of the phase or frequency characteristic of the input signal to the phase or frequency characteristic of the particular one of the one or more reference clock signals by the detector.

Claim 38 was previously cancelled without prejudice.